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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,453	02/08/2002	Luan C. Tran	MI22-1921	1088

21567 7590 07/13/2004

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EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

A

Office Action Summary	Application No.	Applicant(s)	
	10/071,453	TRAN, LUAN C.	
	Examiner	Art Unit	
	Laura M Schillinger	2813	

-- The MAILING DATE of this communication appears on th cover sh et with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-40 and 44-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-40, 44-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 4/1/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 34-36 and 44-46 are rejected under 35 U.S.C. 102(e) as being anticipated by Liaw et al ('276).

In reference to claim 34, Liaw et al ('276) teaches a transistor assembly comprising:

A plurality of active areas having widths defined by STI (Fig.2 (14)) of no greater than one micron, at least some of the widths being different (Fig.2 (14)) (See also Abs., lines: 1-20); and

Gate lines disposed over the plurality of active areas to provide individual transistors, those transistors whose widths are different having different threshold voltages from one another (Fig.s 1 and 2 (13 NMOS and PMOS – see also Fig.4 showing the correlation between channel width and variation in threshold voltage (hereinafter referred to as T_v see also Col.4, lines: 10-25- Table).

In reference to claim 35, Liaw et al ('276) teaches wherein the T_v of at least some transistors are less than one volt (Fig.4 see also Col.4, lines: 10-25- Table).

In reference to claim 36, Liaw et al ('276) teaches wherein individual transistors having active areas with smaller widths have T_v which are smaller than other individual transistors having active areas with larger widths (Fig.4 see also Col.4, lines: 10-25- Table)

In reference to claim 44, Liaw et al ('276) teaches a transistor assembly comprising:

An active area (Fig.2 (12));

A plurality of spaced-apart STI regions received by the active area and defining active sub-areas there between, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is different from the one width (Fig.2 (14) and Abs., lines: 1-20); and

A gate line extending over the one and other sub-area and defining in part, separate transistors, wherein each of the separate transistors has a different T_v (Figs.1 and 2 (13 and 15 NMOS and PMOS, see Figure 4 and see also Col.4, lines: 10-25- Table).

In reference to claim 45, Liaw et al ('276) teaches wherein each active sub-area width of an associated transistor is no greater than about one micron (Abs., lines: 1-20).

In reference to claim 46, Liaw et al ('276) teaches wherein each active sub-area width of an associated transistor is no greater than about one micron, wherein more than two separate transistors have different T_v (Figure 4 and see also Col.4, lines: 10-25- Table).

In reference to claim 47, Liaw et al ('276) teaches wherein each active sub-area width of an associated transistor is no greater than about one micron (Abs., lines: 1-20).

In reference to claim 51, Liaw et al ('276) teaches wherein the gate lines are disposed in a directions over the plurality of the active areas and wherein the widths of the active areas are defined along the direction (Fig.2 (12, 14)).

In reference to claim 52, Liaw et al ('276) teaches wherein the gate lines are disposed in a directions over the one and the other sub-areas and wherein the widths of the sub-areas are defined along the direction (Fig.2 (12, 14)).

In reference to claim 53, Liaw et al ('276) teaches wherein the gate lines are disposed in a directions over the one and the other sub-areas and wherein the widths of the sub-areas are defined along the direction (Fig.2 (12, 14)).

In reference to claim 55, Liaw et al ('276) teaches wherein each active area width of an associated transistor is less than about one micron (Abs., lines: 1-20).

In reference to claim 56, Liaw et al ('276) teaches wherein each active sub-area width of an associated transistor is less than about one micron (Abs., lines: 1-20).

In reference to claim 57, Liaw et al ('276) teaches wherein each active sub-area width of an associated transistor is less than about one micron (Abs., lines: 1-20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 37- 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liaw et al ('276) as applied to claim 34 above, and further in view of Sunouchi et al ('422) and Lu et al ('134).

In reference to claims 38 and 39, Liaw teaches the limitations of the MOS transistor as claimed by the applicant, Sunouchi teaches implementing a similar MOS to make up DRAM circuitry however fails to give specifics of the circuitry to include wherein one transistor comprises a pass transistor nor wherein one of the individual transistors comprises precharge circuitry or a portion of sense amplifier circuitry for a DRAM and has a lower T_v. However, Lu teaches implementing MOS transistors (having STI) in DRAM circuitry wherein one MOS is a pass transistor and another set of MOS transistors is implemented in a sense amplifier for the DRAM (Col.4, lines: 15-45). It would have been obvious to one of ordinary skill in the art to combine the MOS taught by Liaw to be implemented within the DRAM circuitry taught by Sunouchi because Sunouchi teaches the implementation of varied width channel transistors having

minimum element isolation width F within a DRAM (Abs., lines: 1-10), further it would have been obvious to include the pass transistor and. sense amplifier circuitry , and precharge circuitry, taught by Lu within Sunouchi's DRAM circuitry since Lu teaches such circuitry is peripheral circuitry which is typically found within DRAM devices and is further dependent upon T_v (Col.1, lines: 15- 45).

Claim 40, 48-49, 54 and 58-59 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liaw et al ('276) as applied to claim 34 above, and further in view of Sunouchi et al ('422).

In reference to claims 40, Liaw et al ('276) teaches a transistor assembly comprising the elements for claim 34; however fails to teach further comprising a common gate line, which extends over the active area transistors (in parallel configuration) for a DRAM or DRAM circuitry. However, Sunouchi teaches implementing MOS transistors for DRAM circuitry and includes a common gate line formed over parallel transistors having active areas with different widths (Fig.34 (WL)- See also Fig.37(A- STIs 32)). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Liaw's teachings to include a common gate and transistors in parallel configuration because as Sunouchi teaches, common gate lines are used to provide interconnection to transistors implemented within DRAM circuitry (Col.1, lines: 20-25 and Col.4, lines: 55-65, see also Col.10, lines: 10-15).

In reference to claims 49-50, Liaw et al ('276) teaches a transistor assembly comprising:

An active area (Fig.2 (12));

A plurality of spaced-apart STI regions received by the active area and defining active sub-areas there between, individual active sub-areas having respective widths, at least one of the widths being no greater than about one micron and at least one other sub-area having a width which is different from the one width (Fig.2 (14) and Abs., lines: 1-20); and

A gate line extending over the one and other sub-area and defining in part, separate transistors, wherein each of the separate transistors has a different T_v (Figs.1 and 2 (13 and 15 NMOS and PMOS, see Figure 4 and see also Col.4, lines: 10-25- Table) active sub-area width of an associated transistor is no greater than about one micron (Figure 4 and see also Col.4, lines: 10-25- Table).

However fails to teach further comprising a common gate line, which extends over the active area transistors (in parallel configuration) for a DRAM or DRAM circuitry. However, Sunouchi teaches implementing MOS transistors for DRAM circuitry and includes a common gate line formed over parallel transistors having active areas with different widths (Fig.34 (WL)- See also Fig.37(A- STIs 32)). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Liaw's teachings to include a common gate and transistors in parallel configuration because as Sunouchi teaches, common gate lines are used to provide interconnection to transistors implemented within DRAM circuitry (Col.1, lines: 20-25 and Col.4, lines: 55-65, see also Col.10, lines: 10-15).

However, Liaw and Sunouchi fail to teach a pull down circuit coupled to a common node and also fail to teach a sense amplifier formed from a pair of transistors each of the pair having a gate which is cross-coupled to a drain of the pair , sources of the pair coupled to a common node.

Lu et al ('134) teaches a pull down circuit (Fig.2 (pull down control) for application in a DRAM sense amplifier. Lu also teaches a sense amplifier formed from a pair of transistors each of the pair having a gate that is cross coupled to a drain of another of the pair, sources being coupled to the common node (Fig.2 (M 4,5,6,7,8, and 9)). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Liaw's and Sunouchi's teachings to further include pull down circuitry coupled to a common node as taught by Lu in order to activate a sense amplifier (Col.5-6, lines: 65-10). Further Lu asserts that his sense amplifier structure is already well known in the art (Col.5, lines: 50-60).

Response to Arguments

Applicant's arguments filed 9/16/03 have been fully considered but they are not persuasive. Applicant argues that the table of column 4 refers to Fig.3B and not Fig.4, therefore the direction as recited in claim 34 is different and Liaw does not teach a width. The Examiner disagrees with this assertion of prior art teachings because the Liaw reference is clearly referring to a width. The Examiner further finds Applicant's argument that the Liaw reference is obscure such that it disqualifies it as a prior art reference.

Applicant argues that Liaw and Sunouchi in combination with Lu fail to teach precharge circuitry, however Applicant is referred to the Lu reference which is used in combination with Liaw and Sunouchi to reject this limitation (Col.1, lines:.15- 45 and Col.4, lines: 15-45).

Applicant argues that the obviousness rejection made by the Examiner for claims 38 and 39 is not supported by a proper motivational rational- Applicant paraphrases the Examiner's motivational statement and infers that since it is possible to modify the primary reference based on the secondary reference, it is obvious to do so. However, this is not the Examiner's motivation for combining the teachings of Lu and Sunouchi, the Examiner's motivation for combining these references is Lu's teaching that his invention is dependent upon threshold voltage and further is known to have application within DRAM devices. Therefore, Lu's explicit teachings support the Examiner's motivation.

Applicant argues that claim 44 is allowable because the Liaw teaches channel widths, not sub-active areas as claimed by the Applicant. On page 5, lines: 18-21, Applicant defines his active sub-areas as being areas 14 and 16 as depicted in Fig.2. Figure 2 is showing two channel regions defined by STI, which are therefore indistinguishable from Liaw's channel regions.

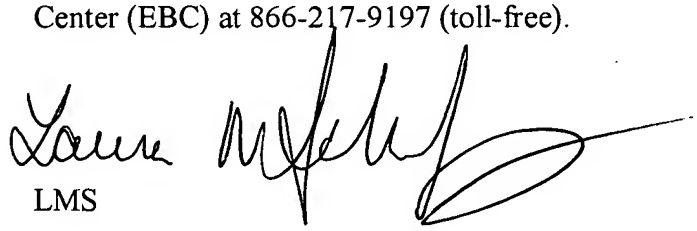
Applicant argues that the pull down circuitry is not connected to a common node as recited in claim 49, however this is not persuasive because the BL as demonstrated in Fig.2 constitutes a common node. Furthermore, Sunouchi teaches implementing MOS transistors for DRAM circuitry and includes a common gate line formed over parallel transistors having active areas with different widths (Fig.34 (WL)- See also Fig.37(A-STIs 32)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



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4/15/04